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(54) Formation of stacked insulation layers in a semiconductor device.

(57) A semiconductor device including a semiconductor substrate (1); a metal wiring layers (31) formed on the semiconductor substrate; a first insulation layer (411) formed on the metal wiring layer (31), the first insulation layer (411) being formed by a tensile stress insulation layer having a contracting characteristic relative to the substrate; and a second insulation layer (412) formed on the first insulation layer (411), the second insulation layer (412) being formed by a compressive stress insulation layer having an expanding characteristic relative to the substrate. The tensile stress insulation layer (411) is produced by thermal chemical vapor deposition or plasma assisted chemical vapor deposition which is performed in a discharge frequency range higher that 2 megahertz; and the compressive stress insulation layer (412) is produced by plasma assisted chemical vapor deposition which is performed in a discharge frequency range lower than 2 megahertz.

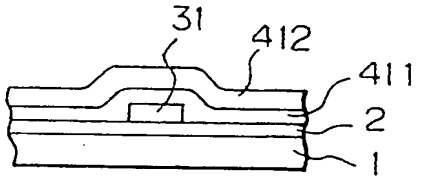

Fig. 5(c)

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A SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME

The present invention relates to a semiconductor device and a method of manufacturing same. More particularly, it relates to a semiconductor device having metal wiring layers and insulation layers formed on the metal wiring layers, and to a method of manufacturing the same.

Generally, in producing a semiconductor device of the above type, the insulation layers formed on the metal wiring layers (e.g., aluminum wiring layers) are produced by chemical vapor deposition using insulation material such as phosphor silicated glass (PSG).

In this method, however, during the formation of the above insulation layers, problems have arisen such as a disconnection of the metal wiring layers due to stress migration due to the effect of stress generated in the insulation layers, and cracks in the insulation layers.

The present invention addresses the above-mentioned problems, and the present invention is concerned with not only the disconnection of the metal wiring layers due to stress migration but also a generation of cracks in the insulation layers.

According to one aspect of the present invention, there is provided a semiconductor device comprising a semiconductor substrate; a metal wiring layer formed over the semiconductor substrate; a first insulation layer formed over the metal wiring layer, the first insulation layer being formed by a tensile stress insulation layer having a contracting characteristic relative to the substrate; and a second insulation layer formed over the first insulation layer, the second insulation layer being formed by a compressive stress insulation layer having an expanding characteristic relative to the substrate.

Also, according to another aspect of the present invention, there is provided a semiconductor comprising a semiconductor substrate; a plurality of metal wiring layers formed over the semiconductor substrate, the plurality of metal wiring layers comprising one or more lower side metal wiring layers having a small wiring width and one or more upper side metal wiring layers having a large wiring width; one or more first insulation layers formed over the respective lower side metal wiring layers , each of the first insulation layers being formed by a tensile stress insulation layer having a contracting characteristic relative to the substrate; and one or more second insulation layers formed over the respective upper side metal wiring layers, each of the second insulation layers being formed by a compressive stress insulation layer having an expanding characteristic relative to the substrate.

According to further aspects of the invention, there are provided methods for manufacturing the above-mentioned semiconductor devices.

In these methods, the or each tensile stress insulation layer is formed by thermal CVD or plasma assisted CVD performed at a discharge frequency higher than around 2 MHz; and the or each compressive stress insulation laver is formed by plasma assisted CVD performed at a discharge frequency lower than 2 MHz.

Reference is made,by way of example, to the accompanying drawings in which:

Figure 1 is a drawing explaining a characteristic of a tensile stress insulation layer;

Fig. 2 is a drawing explaining a characteristic of a compressive stress insulation layer;

Fig. 3 is a drawing showing a tensile stress insulation layer formed on a metal wiring layer as a first insulation layer;

Fig. 4 is a drawing showing a compressive stress insulation layer formed on the first insulation layer as the second insulation layer;

Figs. 5(a) to 5(e) are drawings showing a process for manufacturing a semiconductor device according to a first embodiment of the present invention;

Fig. 6 is a diagram showing how the value of the stress generated in the insulation layer produced by plasma CVD is changed in accordance with the change of discharge frequency used in a plasma CVD system;

Figs. 7(a) to 7(d′) are drawings showing a process for manufacturing semiconductor devices according to second and third embodiments of the present invention;

Figs. 8(a) to 8(h′) are drawings showing a process for manufacturing a semiconductor device according to a fourth embodiment of the present invention;

Fig. 9 is a diagram showing experimental data regarding the generation of stress migration in various cases; and

Fig. 10 is a diagram showing experimental data regarding the generation of cracks in the insulation layers in various cases.

As above-mentioned, a tensile stress insulation layer has a contracting characteristic relative to the substrate, and thus, when the tensile stress insulation layer T is formed on the semiconductor substrate S as shown in Fig. 1, the tensile stress insulation layer T causes the substrate S to bend in a direction such that the insulation layer T contracts relative to the substrate S (i.e. a direction such that the insulation layer T compresses the metal wiring layer M formed on the substrate S).

On the other hand, a compressive stress insulation layer has an expanding characteristic relative to the substrate, and thus, when the compressive stress insulation layer C is formed on the semiconductor substrate S as shown in Fig. 2, the compressive stress insulation layer C causes the substrate S to bend in a direction such that the insulation layer C expands relative to the substrate S (i.e., a direction such that the metal wiring layer M formed on the substrate S is expanded together with the insulation layer C when the metal wiring layer is heated by a current flowing therethrough).

Thus, in embodiments of the first aspect of the invention, by forming the tensile stress insulation layer T on the metal wiring layer M as the first insulation layer, the insulation layer T applies stress to the metal wiring layer M, to compress the metal wiring layer as shown in Fig. 3, and as a result, a disconnection of the metal wiring layer due to stress migration is prevented. Also, by forming the compressive stress insulation layer C on the first insulation layer T as the second insulation layer, as shown in Fig. 4, the compressive stress insulation layer tends to expand together with the expansion of the metal wiring layer when the metal wiring layer is heated, and thus the stress applied by the metal wiring layer to the insulation layer at that time is reduced, and as a result, a generation of cracks in the insulation layer is prevented.

Also, in embodiments of the second aspect of the invention, by forming the tensile stress insulation layers on the respective lower side metal wiring layers having a small wiring width (e.g., on the first and the second metal wiring layers), a disconnection of the metal wiring layers having a small wiring width due to stress migration is prevented. Also, by forming the compressive stress insulation layers on the respective upper side metal wiring layers having a large wiring width (e.g., on the third and the fourth metal wiring layers), generation of cracks in the insulation layers due to the expansion of the metal wiring layers having a large wiring width is prevented. In this connection, with regard to the metal wiring layers having a large wiring width, a disconnection thereof due to stress migration need not be considered.

As described in detail below, the tensile stress insulation layer may be produced by thermal chemical vapor deposition (thermal CVD) or plasma assisted chemical vapor deposition (plasma CVD) performed in a discharge frequency range higher than 2 megahertz. On the other hand, the compressive stress insulation layer may be produced by plasma assisted chemical vapor deposition (plasma CVD) performed in the discharge frequency range lower than 2 megahertz. Also, when the above tensile stress insulation layer or compressive stress insulation layer is formed by a particular plasma assisted chemical vapor deposition such that the above plasma is produced by electron cyclotron resonance (ECR plasma CVD), the surface of the corresponding insulation layer can be made flat, and thus ensure a high reliability of the metal wiring layers formed on the flattened surfaces of the insulation layers.

In this connection, United States Patent 4,446,194 discloses a method of forming a dielectric layer having a compressive stress (corresponding to compressive stress insulation layer) on the metal layer and forming a dielectric layer substantially free of compressive stress (corresponding to the tensile stress insulation layer) on the compressive stress insulation layer, to prevent a formation of voids in the metal layers.

But, as shown in the experimental data described in detail below, a semiconductor device embodying the present invention (i.e., a semiconductor device comprising a tensile stress insulation layer formed on the metal layer and a compressive stress insulation layer formed on the tensile stress insulation layer) may effectively prevent both a disconnection of the metal layers due to stress migration and a generation of cracks in the insulation layers, compared with the device disclosed in the above U.S.P. Namely, in embodiments of the present invention, the above-mentioned particular advantages can be obtained, which cannot be expected from the above U.S.P.

Figures 5(a) to 5(e) show a process for manufacturing a semiconductor device according to a first embodiment of the present invention. First, as shown in Fig. 5(a), a first metal wiring layer (e.g., aluminum wiring layer) 31 is formed on a semiconductor substrate 1 (e.g., a silicon substrate) via a silicon insulation film 2 (e.g., a silicon dioxide (SiO_2) film). Next, as shown in Fig. 5(b), a tensile stress insulation layer 411 is formed as a first insulation layer on the first metal wiring layer 31. The tensile stress insulation layer 411 functions to compress the metal wiring layer 31, due to the contracting characteristic thereof relative to the substrate, and thus prevents stress migration which will cause a disconnection of the metal wiring layer 31. Then, as shown in Fig. 5(c), a compressive stress insulation layer 412 is formed as a second insulation layer on the tensile stress insulation layer 411. In this connection, the compressive stress insulation layer 412 expands together with the metal wiring layer 31 when the metal wiring layer is heated by a current flowing therethrough, due to the expanding characteristic thereof relative to the substrate, and thus stress applied by the metal wiring layer to the insulation layer at that time is reduced, and as a result, generation of cracks in the insulation layer is prevented.

In this connection, the tensile stress insulation

layer 411 can be formed by thermal chemical vapor deposition (thermal CVD) or plasma assisted chemical vapor deposition (plasma CVD). When the thermal CVD method is used, an insulation material such as phosphor silicated glass (PSG) or silicon dioxide (SiO_2) is deposited on the metal wiring layer under the condition of a reduced atmospheric pressure or standard atmospheric pressure, and a processing temperature range higher than 200°C, preferably from 300°C to 450°C. When the plasma CVD method is used, an insulation material (reaction gas) such as the above PSG, SiO_2, SiON, Si_3N_4 or BPSG (boron-phosphor silicated glass), is deposited on the metal wiring layer by supplying a high frequency power having the discharge frequency range higher than 2 megahertz (e.g., 13.56 megahertz) between flat electrodes arranged, for example, in parallel, one of which electrodes is connected to the substrate, under the processing temperature range of from 200°C to 450°C.

The plasma CVD method is used for forming the compressive stress insulation layer 412, and the insulation material (the reaction gas) such as the above PSG, SiO_2, SiON, Si_3N_4, or BPSG is deposited on the first insulation layer by supplying a high frequency power having a discharge frequency range lower than 2 megahertz (e.g., 200 kilohertz) between the above electrodes, under a processing temperature range of from 200°C to 450°C.

Note, the above plasma CVD is of a type other than a plasma CVD wherein the plasma is produced by electron cyclotron resonance (ECR plasma CVD) as described below.

Figure 6 is a diagram showing how the value of the stress generated in the insulation layer produced by the plasma CVD is changed in accordance with a change in the discharge frequency of the high frequency power supplied from a high frequency generator connected between the above electrodes used in the plasma CVD system. In Fig. 6, the abscissa corresponds to the discharge frequency, and the ordinate corresponds to the value of the stress (using 10^n dyne/cm^2, where n = 8 for PSG, and n = 9 for Si_3N_4, as a unit) generated in the insulation layer produced by the plasma CVD. This plasma CVD was performed by using the insulation material (reaction gas) of the above PSG and Si_3N_4. The value of the tensile stress generated in the insulation layer is represented as a positive value, and the value of the compressive stress generated in the insulation layer is represented as a negative value.

The value of the stress becomes zero at the point where the discharge frequency is 2 megahertz, and the value of above tensile stress increases in accordance with the increase of the discharge frequency in the frequency range higher than 2 megahertz. On the other hand, the value of the above compressive stress increases in accordance with a decrease of the discharge frequency in the frequency range lower than 2 megahertz. Namely, the tensile stress insulation layer is formed when the plasma CVD is performed at the discharge frequency range higher than 2 megahertz, and the compressive stress insulation layer is formed at the discharge frequency range lower than 2 megahertz. These conditions remain unchanged even when the above ECR plasma CVD is adopted, instead of another type of plasma CVD, for forming the insulation layer.

Then, as shown in Fig. 5(d), a second metal wiring layer 32 is formed on the second insulation layer 412. When the above-mentioned steps are repeated, a tensile stress insulation layer 421 and a compressive stress insulation layer 422 are successively formed on the second metal wiring layer 32, and a third metal wiring layer 33 is formed on the above insulation layer 422 corresponding to the second insulation layer.

Then, in the above embodiment, the compressive stress insulation layer 432 is formed as a cover on the third metal wiring layer 33, as shown in Fig. 5(e), and subsequently, an anneal processing for the semiconductor device is carried out for about half an hour under a temperature of, for example, 450°C.

Figures 7(a) to 7(d') show a process for manufacturing semiconductor devices according to second and third embodiments of the present invention; the step shown in Fig. 7(a) corresponds to that of the above Fig. 5(a).

Next, in the second embodiment of the present invention, as shown in Fig. 7(b), a tensile stress insulation layer 411' is formed on the first metal layer 31 as the first insulation layer. This insulation layer 411' may be formed by the same means as used to form the tensile stress insulation layer 411 in the first embodiment. Then, as shown in Fig. 7-(c), a compressive stress insulation layer 412' is formed as the second insulation layer on the first insulation layer 411'. The insulation layer 412' is formed so that the surface thereof is made flat.

In this connection, the insulation layer 412' having the flattened surface is formed by the above-mentioned ECR plasma CVD method.

In this case, this ECR plasma CVD is carried out under the condition that the microwave power for producing the ECR Plasma is, for example, 800 watts, and the discharge frequency and the output of the high frequency bias power applied between one electrode connected to the substrate and the other electrode (e.g., the earth electrode) are, for example, 400 kilohertz and 50 to 100 watts, respectively. Namely, as shown in Fig. 6, even when

the above ECR plasma CVD is adopted, the compressive stress insulation layer may be produced in a discharge frequency range of the above bias power which is lower than 2 megahertz. Under this condition, the insulation layer 412′ is produced by using an insulation material such as SiO_2 , PSG, SiON, Si_3N_4 or BPSG.

Accordingly, the surface of the insulation layer 412′ may be flattened, and then, as shown in Fig. 7(d), a second metal wiring layer 32 formed on the flattened surface of the insulation layer 412′. Further, the above steps for forming the first and second insulation layers and the metal wiring layer may be successively repeated a predetermined number of times.

Also, in the third embodiment of the present invention, after the first step shown in Fig. 7(a), as shown in Fig. 7(b′), a tensile stress insulation layer 411″ is formed as the first insulation layer on the first metal wiring layer 31, in such a manner that the surface of the insulation layer 411″ is made flat.

As above-mentioned, the insulation layer 411″ having a flattened surface, is formed by the above ECR plasma CVD method. In this case, this ECR plasma CVD is carried out under the condition that the above microwave power for producing the ECR plasma is, for example, 800 watts, and the discharge frequency and the output of a high frequency bias power applied between the above electrodes, one of which electrodes is connected to the substrate, are, for example, 13.56 megahertz and 50 to 100 watts, respectively. Namely, as shown in Fig. 6, even when the above ECR plasma CVD is adopted, the tensile stress insulation layer may be produced in the discharge frequency range of the above bias power, which is higher than 2 megahertz. Under this condition, the insulation layer 411″ is produced by using the insulation material such as PSG, SiO_2 , SiON, Si_3N_4 or BPSG.

Then, as shown in Fig. 7(c′), a compressive stress insulation layer 412″ is formed as the second insulation layer on the flattened surface of the insulation layer 411″. The insulation layer 412″ may be formed by the same means used to form the compressive stress insulation layer 412 in the first embodiment. The surface of the insulation layer 412″, which is formed on the flattened surface of the insulation layer 411″ also may be flattened. Then, as shown in Fig. 7(d′), a second metal wiring layer 32 is formed on the flattened surface of the insulation layer 412″. Further, the above steps for forming the first and second insulation layers and the metal wiring layer can be successively repeated a predetermined number of times.

Thus, according to the second and third embodiments of the present invention, since each of the metal wiring layers is formed on the flattened surface of the corresponding insulation layer, a high reliability of the metal wiring layers is ensured.

Figures 8(a) to 8(h′) show a process for manufacturing a semiconductor device according to a fourth embodiment of the present invention. In this embodiment, a plurality of metal wiring layers are provided, a tensile stress insulation layer is formed on each of lower side metal wiring layers having a small wiring width, and a compressive stress insulation layer is formed on each of upper side metal wiring layers having a large wiring width.

Namely, in this embodiment, the tensile stress insulation interlayers 41 and 42 are formed on the first and second metal wiring layers 31 and 32 having small wiring widths ℓ_1 and ℓ_2 , respectively, to prevent disconnection of the metal wiring layers having the small wiring widths due to stress migration. In this connection, the tensile stress insulation layers may be formed by the same means used to form the tensile stress insulation layers in the above first embodiment.

Also, the compressive stress insulation layers (interlayers and a cover) 43, 44, and 45 are formed on the third, fourth, and fifth metal wiring layers 33, 34, and 35 having large wiring widths ℓ_3 , ℓ_4 , and ℓ_5 , respectively. In this connection, it is not necessary to consider disconnection of the metal wiring layers having the large wiring widths ℓ_3 to ℓ_5 , due to stress migration. Accordingly, as above-mentioned, the compressive stress insulation layers are formed on the metal wiring layers having the large wiring widths, to prevent the generation of cracks in the insulation layers, due to expansion of the metal wiring layers having the large wiring widths. The compressive stress insulation layers also may be formed by the same means used to form the compressive stress insulation layers in the above first embodiment.

In this connection, in the above semiconductor device having a plurality of metal wiring layers, one or more metal wiring layers having the small wiring widths (e.g., signal lines) are formed with a high wiring density as the lower side metal wiring layers (in the above case, as the first and second metal wiring layers), and the remaining metal wiring layers having the large wiring widths (e.g., power supply lines) are formed with a low wiring density as the upper side metal wiring layers (in the above case, as the third to fifth metal wiring layers).

In Figs. 8(a) to 8(h′), the steps shown in Fig. 8-(a) and Fig. 8(b) correspond to those of Fig. 5(a) and Fig. 5(b), respectively.

Next, as shown in Fig. 8(c), the second metal wiring layer 32 having the wiring width ℓ_2 is formed on the tensile stress insulation interlayer 41, and as shown in Fig. 8(d), the tensile stress insulation interlayer 42 is again formed on the metal wiring layer 32. Next, as shown in Fig. 8(e), the third metal wiring layer 33 having the wiring width ℓ_3 ,

which is larger than the above ℓ_1, and ℓ_2, is formed on the insulation interlayer 42, and as shown in Fig. 8(f), the compressive stress insulation interlayer 43 is then formed on the metal wiring layer 33. Next, as shown in Fig. 8(g), the fourth metal wiring layer 34 having the wiring width ℓ_4, which is also larger than ℓ_1, and ℓ_2, is formed on the insulation interlayer 43. The above steps are repeated a predetermined number of times, and finally, as shown in Fig. 8(h), the compressive stress insulation layer 45 is formed as the cover on the fifth metal wiring layer 35 having, for example, the wiring width ℓ_5 which is also larger than ℓ_1, and ℓ_2.

Figure 8(h') shows another typical construction of the semiconductor device according to the above fourth embodiment of the present invention. This semiconductor device comprises four metal wiring layers including two lower side metal wiring layers (i.e., the first and second metal wiring layers 31 and 32 having small wiring widths ℓ_1' and ℓ_2', respectively) and two upper side metal wiring layers (i.e., the third and fourth metal wiring layers 33 and 34 having large wiring widths ℓ_3' and ℓ_4', respectively). The tensile stress insulation interlayers 41 and 42 are formed on the above lower side metal wiring layers 31 and 32, respectively, and the compressive stress insulation layers (an interlayer and a cover) 43 and 44 are formed on the above upper side metal wiring layers 33 and 34, respectively. The tensile stress insulation layers and the compressive stress insulation layers may be formed by the same means used to form the tensile stress insulation layers and the compressive stress insulation layers in the above first embodiment.

Figure 9 shows experimental data regarding the generation of the above stress migration in various cases. The data was obtained under the condition that a current having a density of 3.0×10^5 A/cm^2 (Amperes/cm^2) is made to flow through the aluminum wiring layers having a wiring width of 1.5 μ (microns) and a wiring thickness of 0.7 μ (microns), at a temperature of 250° C.

In Fig. 9, the abscissa corresponds to the test time, (in hours), and the ordinate corresponds to an accumulated ratio of the generation of the defect (i.e., the above stress migration), shown as a percentage.

In Fig. 9, marks "•" along a line "C" correspond to test data in the case wherein each of the insulation interlayers is formed only by the tensile stress insulation layer produced by thermal CVD, and marks "o" along a line "d" correspond to test data in the case wherein each of the insulation interlayers is formed only by the compressive stress insulation layer produced by plasma CVD. Further, marks "□" along a line "b" correspond to test data in the case wherein each of the insulation interlayers comprises the compressive stress insulation layer as the first insulation layer and the tensile stress insulation layer formed on the compressive stress insulation layer as the second insulation layer, as shown in the above U.S.P. 4,446,194, and marks "Δ" along a line "a" correspond to test data in the case wherein each of the insulation interlayers comprises the tensile stress insulation layer as the first insulation layer and the compressive stress insulation layer formed on the tensile stress insulation layer as the second insulation layer, as in the present invention.

As shown in Fig. 9 it is apparent that a construction embodying the present invention can be remarkably effective for preventing stress migration, compared to other cases.

Figure 10 shows experimental data regarding the generation of cracks in the insulation layers in various cases.

In Fig. 10, test data I corresponds to the case wherein the insulation interlayers formed on the first, second, and third metal wiring layers are all formed only by the tensile stress insulation layers T, and only the cover formed on the fourth metal wiring layer is formed by the compressive stress insulation layer C. Also, test data III corresponds to the case wherein the insulation interlayers formed on the first and second metal wiring layers are formed only by the tensile stress insulation layers T, and the insulation interlayer formed on the third metal wiring layer comprises the compressive stress insulation layer C as a first insulation layer 3-1 of the corresponding insulation interlayer and the tensile stress insulation layer T formed on the first insulation layer 3-1 as a second insulation layer 3-2 of the corresponding insulation interlayer, as shown in the above U.S.P., and the cover formed on the fourth metal wiring layer is formed by the compressive stress insulation layer C. These test data I and III show that, according to the above constructions, it is impossible to prevent the generation of cracks in the insulation layers, as shown by marks "X".

On the other hand, test data II corresponds to the case wherein the insulation interlayers formed on the first and second metal wiring layers (i.e., the metal wiring layers having the small wiring width) are formed by the tensile stress insulation layers T, and the insulation interlayer formed on the third metal wiring layer and the cover formed on the fourth metal wiring layer (i.e., the insulation interlayer and the cover formed on the metal wiring layers having the large wiring width) are formed by the compressive stress insulation layers C, as shown in the fourth embodiment of the present invention. Also, test data IV corresponds to the case wherein the insulation interlayer formed on

the first metal wiring layer is formed by the tensile stress insulation layer T, and each of the insulation interlayers formed on the second and third metal wiring layers comprises the tensile stress insulation layer T as a first insulation layer 2-1 or 3-1 of the corresponding insulation interlayer and the compressive stress insulation layer C formed on the first insulation layer 2-1 or 3-1 as a second insulation layer 2-2 or 3-2 of the corresponding insulation interlayer, as shown in the first embodiment of the present invention, and the cover formed on the fourth metal wiring layer is formed by the compressive stress insulation layer C. Further, test data V corresponds to the case wherein each of the insulation interlayers formed on the first, second, and third metal wiring layers comprises the tensile stress insulation layer T as a first insulation layer 1-1, 2-1, or 3-1 of the corresponding insulation interlayer and the compressive stress insulation layer C formed on the first insulation layer 1-1, 2-1, or 3-1 as a second insulation layer 1-2, 2-2, or 3-2 of the corresponding insulation interlayer, as shown in the first embodiment of the present invention, and the cover formed on the fourth metal wiring layer is formed by the compressive stress insulation layer C. These test data II, IV, and V show that, according to these embodiments of the present invention, the generation of cracks in the insulation layers can be effectively prevented, as shown by marks "o".

Claims

1. A semiconductor device comprising:
a semiconductor substrate;
a metal wiring layer formed over side semiconductor substrate;
a first insulation layer formed over said metal wiring layer, said first insulation layer being formed by a tensile stress insulation layer having a contracting characteristic relative to said substrate; and
a second insulation layer formed over said first insulation layer, said second insulation layer being formed by a compressive stress insulation layer having an expanding characteristic relative to said substrate.

2. A method of manufacturing a semiconductor device, comprising steps of:
forming a metal wiring layer over a semiconductor substrate;
forming a first insulation layer over said metal wiring layer by thermal chemical vapor deposition or plasma assisted chemical vapor deposition which is performed in a discharge frequency (range)higher than 2 megahertz; and
forming a second insulation layer over said first insulation layer by plasma assisted chemical vapor deposition which is performed in a discharge frequency (range)lower than 2 megahertz.

3. A method of manufacturing a semiconductor device according to claim 2, wherein at least one of said first and second insulation layers is formed by plasma assisted chemical vapor deposition in which said plasma is produced by electron cyclotron resonance.

4. A semiconductor device comprising:
a semiconductor substrate;
a plurality of metal wiring layers formed over said semiconductor substrate, said plurality of metal wiring layers comprising one or more lower side metal wiring layers having a small wiring width and one or more upper side metal wiring layers having a large wiring width;
one or more first insulation layers formed over the respective lower side metal wiring layers, each of said first insulation layers being formed by a tensile stress insulation layer having a contracting characteristic relative to said substrate; and
one or more second insulation layers formed over the respective upper side metal wiring layers, each of said second insulation layers being formed by a compressive stress insulation layer having an expanding characteristic relative to said substrate.

5. A semiconductor device according to claim 4, wherein said lower side metal wiring layers are used as signal lines and said upper side metal wiring layers are used as power supply lines.

6. A semiconductor device according to claim 4, wherein the number of said plurality of metal wiring layers is four, among which metal wiring layers, first and second metal wiring layers are formed as said lower side metal wiring layers, and third and fourth metal wiring layers are formed as said upper side metal wiring layers.

7. A method of manufacturing a semiconductor device, comprising steps of:
forming a plurality of metal wiring layers over a semiconductor substrate, said plurality of metal wiring layers comprising one or more lower side metal wiring layers having a small wiring width and one or more upper side metal wiring layers having a large wiring width;
forming one or more first insulation layers over respective lower side metal wiring layers by thermal chemical vapor deposition or plasma assisted chemical vapor deposition which is performed in a discharge frequency (range) higher than 2 megahertz; and
forming one or more second insulation layers over respective upper side metal wiring layers by plasma assisted chemical vapor deposition which is performed in a discharge frequency (range) lower than 2 megahertz.

8. A method of manufacturing a semiconductor device according to claim 7, wherein a number of said plurality of metal wiring layers is four, among which metal wiring layers, first and second metal wiring layers are formed as said lower side metal wiring layers, and third and fourth metal wiring layers are formed as said upper side metal wiring layers.

Fig. 1

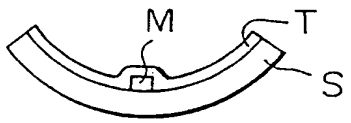

Fig. 2

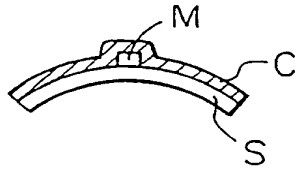

Fig. 3

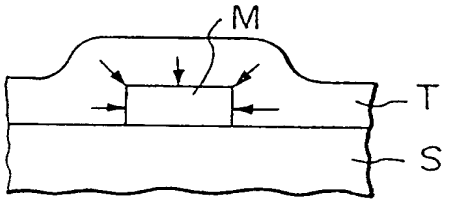

Fig. 4

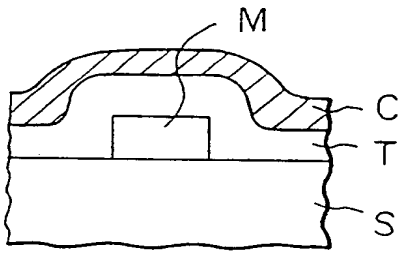

Fig. 6

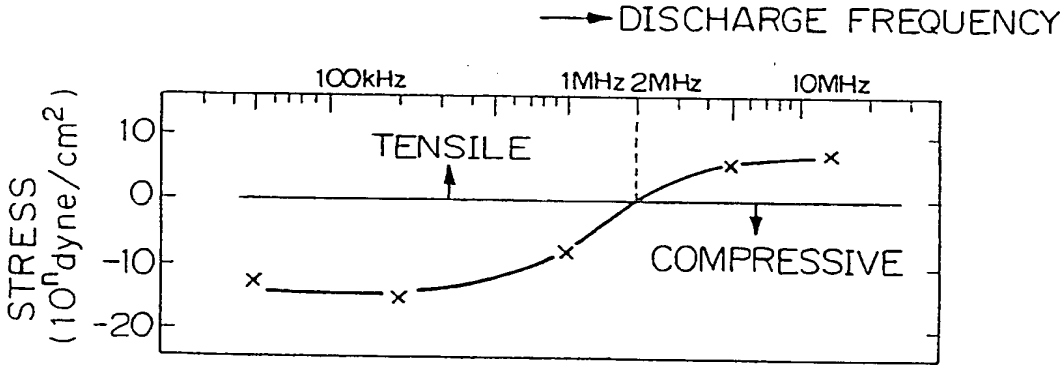

Fig. 5(a)

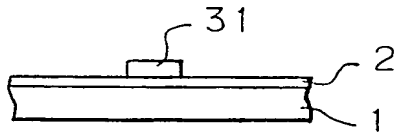

Fig. 5(b)

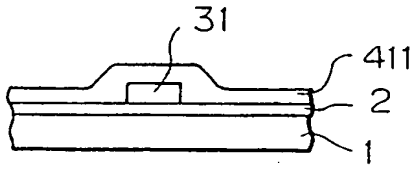

Fig. 5(c)

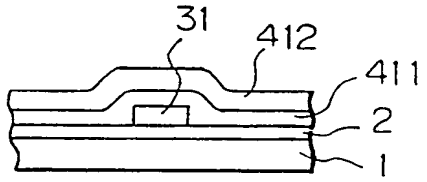

Fig. 5(d)

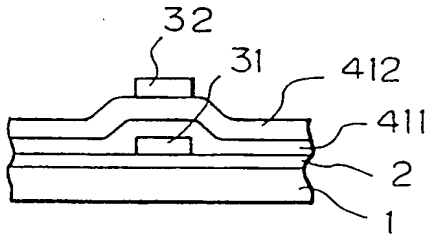

Fig. 5(e)

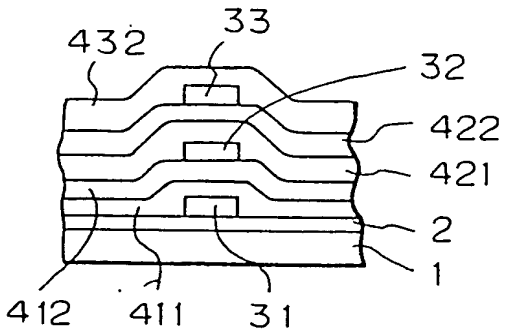

Fig. 7(a)

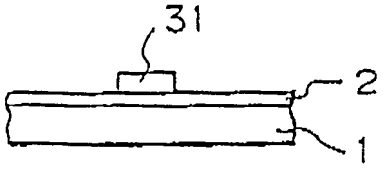

Fig. 7(b)

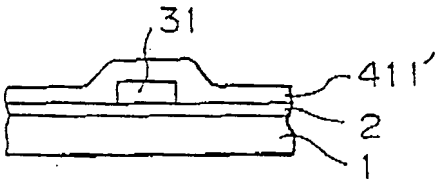

Fig. 7(b')

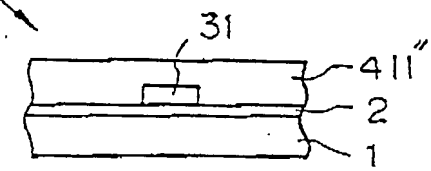

Fig. 7(c)

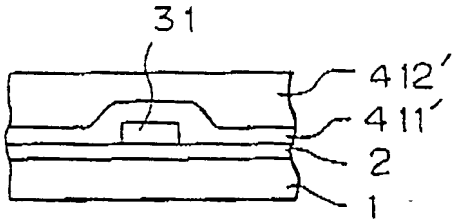

Fig. 7(c')

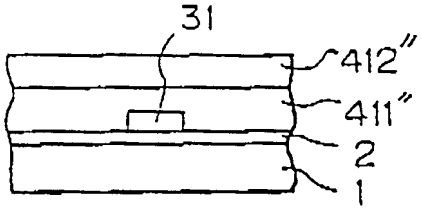

Fig. 7(d)

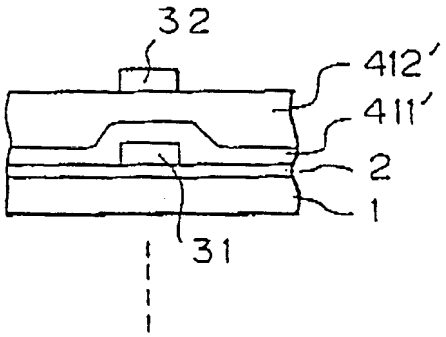

Fig. 7(d')

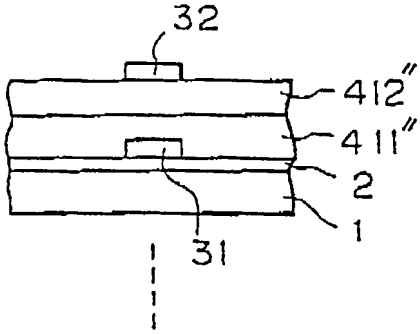

Fig. 8 (a)

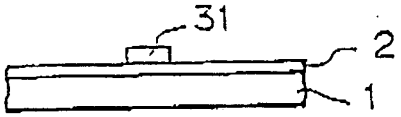

Fig. 8 (b)

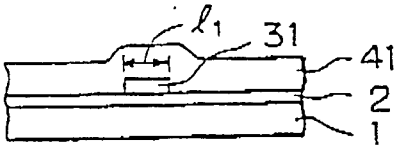

Fig. 8 (c)

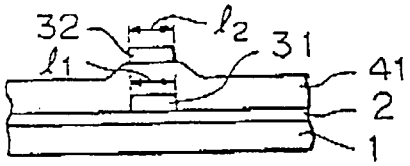

Fig. 8 (d)

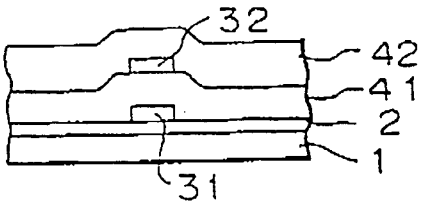

Fig. 8 (e)

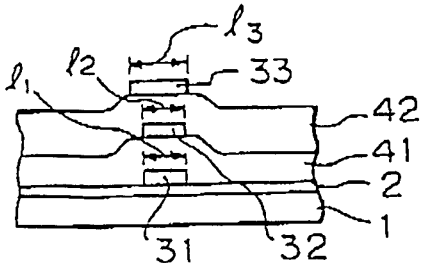

Fig. 8 (f)

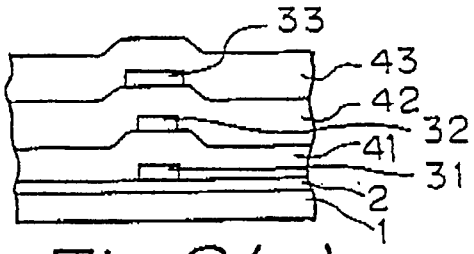

Fig. 8 (g)

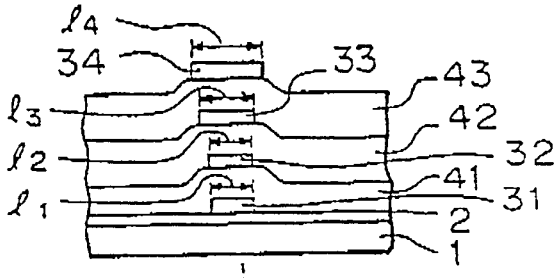

Fig. 8 (h)

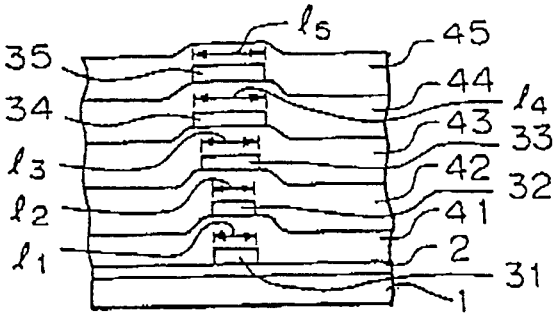

Fig. 8 (h')

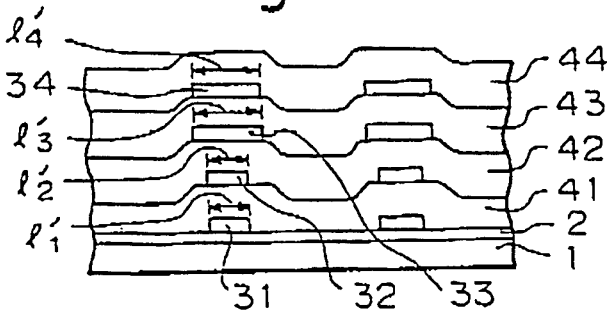

Fig. 9

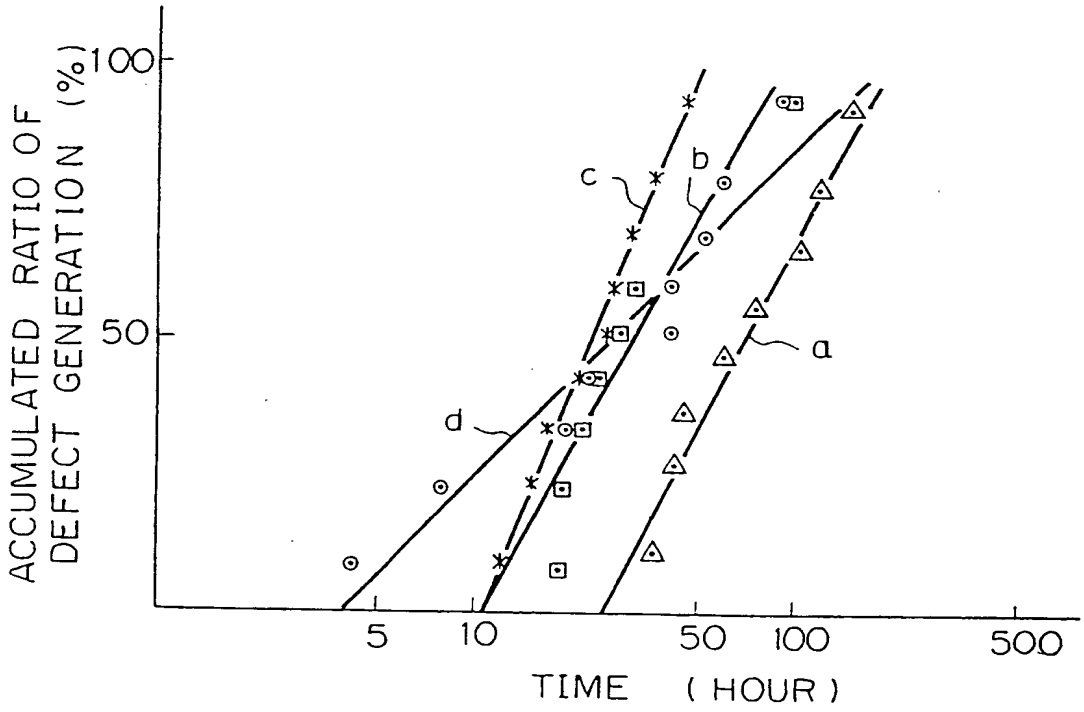
ACCUMULATED RATIO OF DEFECT GENERATION (%)
100
50
5
10
50
100
500
TIME (HOUR)
a
b
c
d

Fig. 10

INSULATION INTERLAYERS AND COVER / TEST DATA	1-1	1-2	2-1	2-2	3-1	3-2	COVER	GENERATION OF CRACKS
I	T	T	T	T	T	T	C	X
II	T	T	T	T	C	C	C	○
III	T	T	T	T	C	T	C	X
IV	T	T	T	C	T	C	C	○
V	T	C	T	C	T	C	C	○

EP 0 307 099 A1

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EUROPEAN SEARCH REPORT

Application Number

EP 88 30 7623

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	PATENT ABSTRACTS OF JAPAN, vol. 6, no. 119 (E-116)[997], 3rd July 1982; & JP-A-57 45 931 (FUJITSU K.K.) 16-03-1982 * Abstract *	1,2	H 01 L 21/318// H 01 L 21/90
A	IDEM ---	3,4,7	
A	PATENT ABSTRACTS OF JAPAN, vol. 11, no. 138 (E-503)[2585], 2nd May 1987; & JP-A-61 279 132 (SONY CORP.) 09-12-1986 * Abstract * ---	4,7	
A	PLASMA CHEMISTRY & PLASMA PROCESSING, vol. 7, no. 1, March 1987, pages 109-124, Plenum Publishing Corp., Bristol, GB; W.A.P. CLAASSEN: "Ion bombardment-induced mechanical stress in plasma-enhanced deposited silicon nitride and silicon oxynitride films" * Figure 1; page 111, line 4 - page 114, line 4 from the bottom; page 120, line 12 - page 122, line 10 * ---	1,2,4,7	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L
A	JAPANESE JOURNAL OF APPLIED PHYSICS. SUPPLEMENTS, 17TH CONERENCE ON SOLID STATE DEVICES AND MATERIALS, 25th-27th August 1985, pages 329-332, Tokyo, JP; K. MACHIDA et al.: "New planarization technology using Bias-ECR plasma deposition" * Figure 2; page 330, right-hand column, paragraph "IV. Characteristics of Bias-ECR Plasma Deposition" * --- -/-	3	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-11-1988	MACHEK,J.

CATEGORY OF CITED DOCUMENTS

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EUROPEAN SEARCH REPORT

Application Number

EP 88 30 7623

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EXTENDED ABSTRACTS, vol. 87-1, no. 1, Spring 1987, pages 366-367, no. 254, Philadelphia, PA, US; M. DOKI et al.: "ECR plasma CVD of insulator films - low temperature process for ulsi -" * Whole article *	3	
A	PATENT ABSTRACTS OF JAPAN, vol. 11, no. 390 (E-567)[2837], 19th December 1987; & JP-A-62 154 642 (MATSUSHITA ELECTRONICS CORP.) 09-07-1987 * Abstract *	4,7	
P,A	EP-A-0 252 179 (IBM) * Abstract; figure 1; claims 1,3,8 *	1,2	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-11-1988	MACHEK,J.

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